

Multi Threshold CMOS Leakage Reduction Technique

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ABSTRACT

Now a day it is a difficult to design a low power digital circuit, as the scaling increases the leakage power increases. So we are using many types of power gating techniques and to provide a better power efficiency by removing these kinds of leakages. In this paper, a variety of leakage power suppression techniques that allow further scaling of CMOS integrated circuits are introduced. The widely employed multi-threshold CMOS (MTCMOS) circuit technique, which is also known as Power/ground gating technique, is effective in reducing leakage power consumption of a circuit block in idle (SLEEP) mode.

Keywords- Leakage power, Multi-threshold CMOS, Sleep mode, Standby mode.

1. INTRODUCTION

One of the most important issues in VLSI design is leakage power with continuous down scaling in advanced CMOS technology. There are three different approaches for semiconductor technology scaling: constant voltage scaling, constant field scaling, and generalized scaling. The first method is Constant voltage scaling that was widely employed in semiconductor industry. The device dimensions are scaled down by a factor of “S”, With the constant voltage scaling and the doping concentration of the channel is increased by a factor of “S²”. Here, provided the supply voltage is constant from one generation technology to the next. The electric field in a scaled MOS transistor is increased by a factor of “S”, which is increasing the carrier velocity. However, the elevated electric field reduces the reliability of the scaled MOS transistor. MTCMOS technology has provided with alternate way to build logic gates operating at a high speed and provided relatively small power dissipation as compared to traditional CMOS. MTCMOS is an effective circuit-level technique that provides a high performance and very low-power design by utilizing both low and high-threshold voltage transistors.

2. SOURCES OF POWER DESSIPATION

The major sources of power dissipation in CMO based digital circuit can be summarized as follows.

i. Dynamic Power Dissipation

When logic transition occurs, current flows from V_{DD} to GND. Dynamic power is dissipated during charging/discharging process of the capacitances. The power is dissipated by charging the various load capacitances whenever they are switched. In CMOS logic, when one cycle is completed, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge:

$$P = CV^2f$$

At every clock cycle, most of gates do not switch, since they are often accompanied by a factor α , which is also known as activity factor. Now, the dynamic power dissipation can be written as:

$$P = \alpha CV^2f$$

ii. Static Power Dissipation

Static power dissipation occurs during the current flows from V_{DD} to GND regardless of logic transition. It has three components, (a) Tunneling current through gate, (b) Leakage current through reverse biased diodes and (c) Sub-threshold condition when the transistors are off oxide

iii. Short circuit Power Dissipation

Since there is a finite rise/fall time for both PMOS and NMOS during transition from off to on, current will find a path directly from V_{DD} to ground, hence creating a short circuit current. Short circuit power dissipation increases with rise and fall time of the transistors.

3. POWER GATING AND MULTI-THRESHOLD CMOS

We can achieve a lower threshold voltage with the MTCMOS circuit technology and therefore, higher performance as well as smaller leakage current. The is an efficient way of lowering the leakage power dissipation of a VLSI circuit.

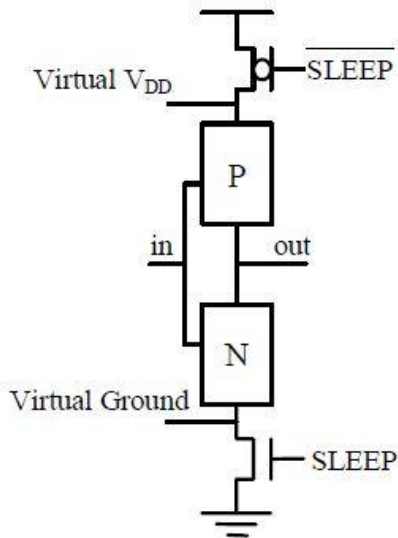


Figure 1: Power gating structure.

This can be achieved by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply as depicted in Figure 1. In practice, it is noticed that only one transistor is necessary. Because of their lower on-resistance, usually NMOS transistors are used. The sleep transistor is on in the ACTIVE state. Therefore, the circuit functions as usual. In the STANDBY state, the transistor is turned off, which disconnects the gate from the ground. The threshold voltage of the sleep transistor must be large to reduce the leakage. Otherwise, the leakage current is high in sleep transistor, which will make the power gating less effective. In practice, Multi-Threshold CMOS (MTCMOS) is used for power gating. In these technologies there are several types of transistors with different V_T values. Transistors with a low V_T are used to implement the logic, while high- V_T devices are used as sleep transistors. For the proper functionality of the circuit, the sleep transistor has to be carefully sized to reduce its voltage drop while it is on. The voltage drop on the sleep transistor reduces the effective supply voltage of the logic gate. Also, due to the body effect, it enhances the threshold of the pull-down transistors. But, this increases the high-to-low transition delay of the circuit. This problem can be solved by using a large

sleep transistor. But, using a large sleep transistor increases the area overhead and the dynamic power consumed for turning the transistor on and off. It is not possible to save power for short idle periods because of this dynamic power consumption.

Since there is a use of one transistor for each logic gate results in a large area and power overhead, one transistor may be used for each group of gates as depicted in Figure 2. It is noticed that the size of the sleep transistor in this figure 2 is to be larger than the one used in Figure 1. It is necessary to find the vector that causes the worst case delay in the circuit to obtain the optimum size of the sleep transistor. This requires simulating the circuit under all possible input values, a task that is not possible for large circuits.

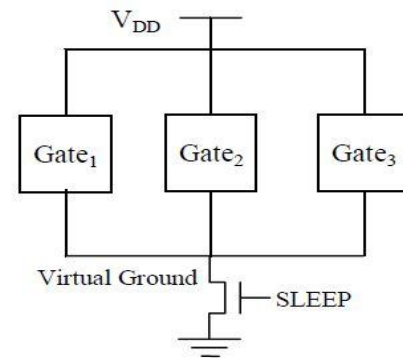


Figure 2: Using one sleep transistor for several gates.

The existing design of XNOR gate is shown in Fig.3, consists of 3 transistors as one pMOS and two nMOS.

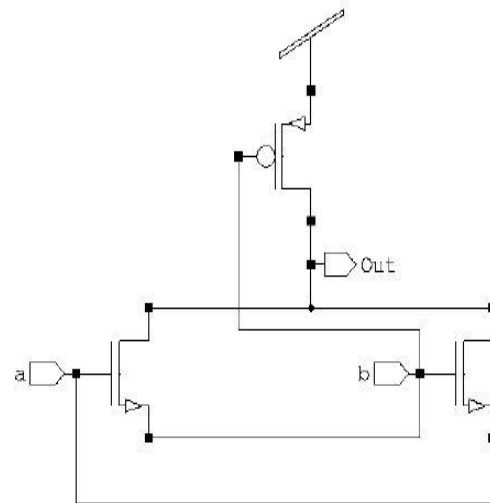


Figure 3: Schematic diagram of existing XNOR gate

When $ab=00$, both nMOS are OFF and pMOS is ON. As pMOS is strong '1' device it will pass complete logic "high" signal at the output.

When $ab=01$, one nMOS is OFF and other nMOS is ON. As nMOS is strong '0' device it will pass complete logic "low" signal at the output.
 When $ab = 10$, nMOS (second) and pMOS are ON. As mobility of nMOS is nearly three times greater than pMOS, hence it will drive the output ignoring the effect of ON pMOS transistors which results into zero output.
 When $ab=11$, both the nMOS transistors are ON and only nMOS will be responsible for driving the output.

Fig.4 shows the schematic of proposed 3T XNOR gate with MTCMOS technique.

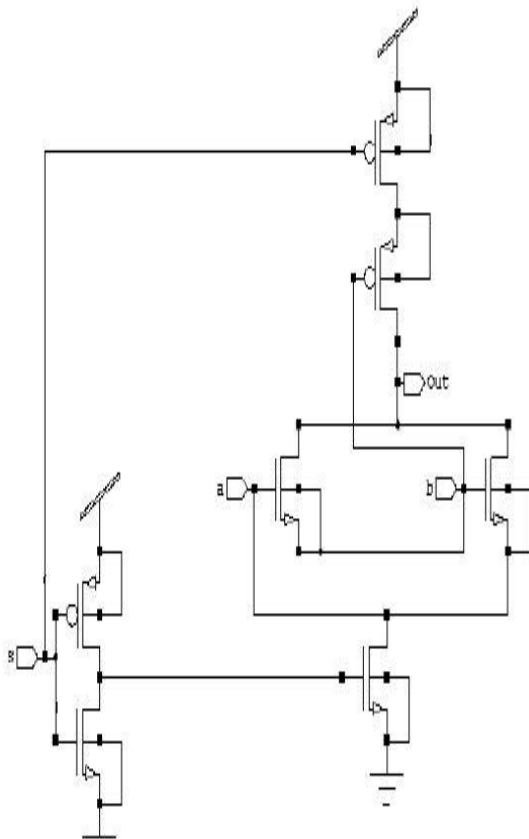


Figure 4: Schematic diagram of proposed XNOR gate with MTCMOS.

4. SIMULATION RESULTS

All schematic simulations have been performed on Tanner EDA tool with input voltage ranging from 0.4V to 1V in steps of 0.1V. To establish an impartial testing environment both circuit have been tested on the same input patterns which covers all combinations of the input stream.

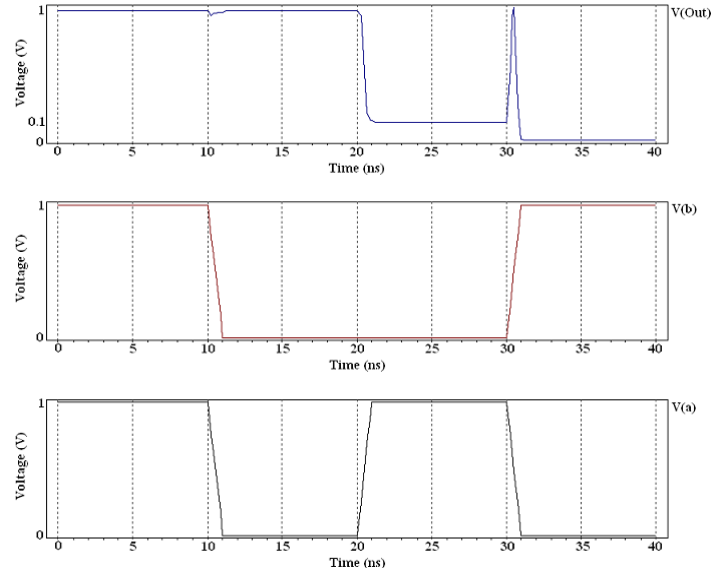
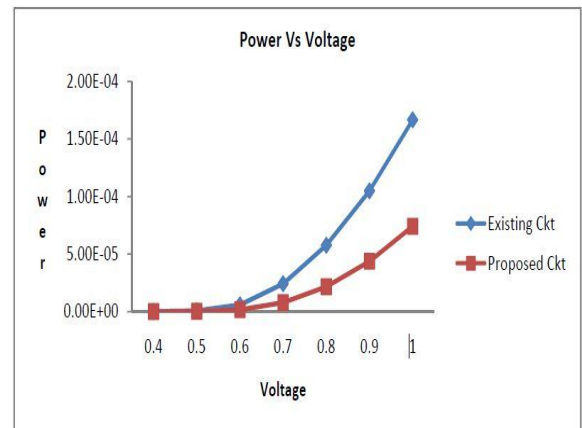


Figure 5: Input-output waveform of proposed Circuit.

Power consumption with varying supply voltage



5. CONCLUSION

The XNOR gate with MTCMOS gives the better performance than the existing XNOR gate. It has been tested to have better temperature sustainability and significantly less power and power-delay product at various input voltages and frequencies. MTCMOS circuit has a marginal increase in area compared to the CMOS circuit; overall, we achieved the lowest power dissipation with MTCMOS technique.

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